

```

0001  *H TSTMEM
0002
0003  ;-----
0004  ;***** R.M.L. MEMORY DIAGNOSTIC *****
0005  ;-----
0006  ;-----
0007
0008  ;THE MEMORY LIMITS FOR THE TEST ARE SET BY PARAMETERS
0009  ;'RAM' AND 'TOP'. 'RAM' IS THE ADDRESS OF THE FIRST
0010  ;LOCATION TESTED; 'TOP' IS THE MORE SIGNIFICANT
0011  ;BYTE OF (THE LAST ADDRESS + 1).
0012
0013  RAM      EQU      4140H      ;START TEST HERE
0014  TOP      EQU      80H       ;FOR 16 K BYTES
0015
0016                ORG      4100H
0017
0018  START:   LD        DE.0      ;CLEAR PASS CNTR
0019
0020  PASS:    LD        B.0       ;INIT PATTERN MODIFIER
0021
0022  CYCLE:   LD        HL,RAM     ;HL -> START OF RAM TO TEST
0023
0024  FILL:    LD        A,L        ;CONSTRUCT PATTERN
0025                XOR        H      ; FROM ADDRESS
0026                XOR        B      ; AND MODIFIER
0027                LD        (HL),A   ;FILL MEMORY
0028                INC        HL
0029                LD        A,H      ;REPEAT FILL LOOP
0030                CP        TOP      ; UNTIL ALL LOCATIONS
0031                JR        NZ,FILL  ; HAVE BEEN FILLED
0032
0033                LD        HL,RAM   ;RESET START ADDR
0034  TEST:    LD        A,L        ;RECONSTRUCT PATTERN
0035                XOR        H
0036                XOR        B
0037                CP        (HL)     ;COMPARE MEMORY
0038                JR        Z,$+3    ;IF IT MATCHES
0039                DEFB        BREAK  ;ELSE HALT
0040                INC        HL
0041                LD        A,H
0042                CP        TOP
0043                JR        NZ,TEST  ;RPT UNTIL ALL TESTED
0044
0045  ;CYCLE COMPLETE
0046
0047                LD        A,'/'    ;INDICATE ACTIVITY
0048                EMT        OUTC
0049                EMT        KBDIN   ;CHECK FOR CONTROL C
0050                INC        B       ;CHANGE MODIFIER AND RPT
0051                JR        NZ,CYCLE ;UNTIL PASS COMPLETE
0052
0053  ;PASS COMPLETE - OUTPUT PASS COUNT AND CONTINUE
0054

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412B 3E0D      0055      LD      A,CR
412D F701      0056      EMT     OUTC
412F 21C10D    0057      LD      HL,0DC1H      ;VT BOTTOM LINE, COL 2
4132 13        0058      INC     DE
4133 F70B      0059      EMT     OPNWT      ;OPEN VT MEMORY
4135 F714      0060      EMT     DEOUT     ;WRITE PASS NUMBER
4137 F70C      0061      EMT     CLOSE    ;CLOSE VT MEMORY
4139 3E0D      0062      LD      A,CR
413B F701      0063      EMT     OUTC
413D 18C4      0064      JR      PASS      ;CONTINUE TESTING
          0065
          0066      ;LINKS TO COS 2.2
          0067
0001      0068      OUTC     EQU      1
0002      0069      KBDIN    EQU      2
000B      0070      OPNWT    EQU      0BH
000C      0071      CLOSE    EQU      0CH
0014      0072      DEOUT    EQU      14H
00FF      0073      BREAK    EQU      0FFH      ;BREAKPOINT CODE (RST 38H)
000D      0074      CR       EQU      0DH      ;ASCII CARRIAGE RETURN
          0075
          0076      END

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SYMBOL TABLE:

BREAK	00FF	CLOSE	000C	CR	000D	CYCLE	4105
DEOUT	0014	FILL	4108	KBDIN	0002	OPNWT	000B
OUTC	0001	PASS	4103	RAM	4140	START	4100
TEST	4115	TOP	0080				

NO ERRORS

MEMORY DIAGNOSTIC

File name	TSTMEM
Memory limits	4100 to 413E
Start address	4100

1. DESCRIPTION

This program tests random access memory (RAM). Since the COS monitor relies on the integrity of a small area of RAM (between addresses 4000 to 40FF, inclusive), a gross memory fault will result in the failure of the system to work at all. Less catastrophic errors may be picked up by use of the 'front panel' fill and test memory command (P) or by the failure of the monitor to set location 'HIMEM' correctly after a system reset (HIMEM normally contains the address of highest available memory in the contiguous block starting at 4000).

TSTMEM carries out a much more thorough memory test than these simple functions. Memory is filled with a pseudo-random bit pattern, then the content is compared with the value which was loaded. A 'pass' is complete when each byte has been tested with all 256 possible patterns.

During each fill and compare cycle, of which there are 256 in a pass, a test pattern for each byte is constructed from the exclusive - OR of a constant, the low byte and the high byte of its address. Thus each byte within a memory 'page' of 256 locations receives a different pattern and the order of test patterns between pages varies. In this way errors in which bits

are 'stuck' at either 0 or 1 and interactions within a byte are readily detected. All memory is written before being tested to detect address interaction.

Activity is indicated during each cycle by the printing of a slash (/); at the end of a successful pass TSTMEM prints the pass number, then begins another. Testing continues until an error is detected or CONTROL C is typed. A pass takes approximately 2½ minutes for 16K bytes of RAM.

If an error is detected, TSTMEM halts with a breakpoint at location 411B. Register pair HL points to the byte in which the error has been detected (with its content displayed further along the HL row of the register section of the front panel), while Register A contains the expected pattern. Register pair DE contains the pass number. To carry on testing after an error has been detected, enter 411C into the program counter (411C.) and continue (K).

2. OPERATION

As distributed, TSTMEM is set up for a 16K byte memory. If this differs from the memory size of your system, halt the program with CONTROL C and use the front panel commands to modify the content of addresses 410F and 411F to the appropriate value for your memory size. This should be the more significant byte of the address of the location one higher than the highest address to be tested, viz:

Memory size	Value
-------------	-------

4K	50
----	----

8K	60
----	----

12K	70
-----	----

Memory size	Value
(16K	80)
20K	90
24K	A0
28K	B0
32K	C0 etc.

(These values must lie on a memory page boundary)

The address from which TSTMEM begins testing is in locations 4106/7 and 4113/4. This can be changed from the current setting of 4140 if required (note that the address is, as usual, stored with the less significant byte first). After modification, TSTMEM can be saved on tape ready for immediate use, or restarted at address 4100.

With adjustment of these two parameters (i.e. of the address range within which the test is carried out) TSTMEM is position independant and can be run at any address. It does not itself use any memory addresses other than those which contain the program code, but it does communicate with the user via various monitor trap calls, which make use of monitor RAM.